IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Number	:	7,039,118 B1	Issued: May 2, 2006
Application Number	:	09/761,211	Confirmation No.: 5490
Applicant	:	Para K. Segaram	
Filed	:	January 16, 2001	
Group Art Unit	:	2631	
Examiner	:	Kevin Michael Burd	

MAIL STOP CERTIFICATE OF CORRECTION
Commissioner for Patents
P.O. Box 1450
Alexandria, VA. 22313–1450

Request For Certificate Of Correction Of Patent Under 37 C.F.R. 1.323

Sir:

Patentees request a Certificate of Correction to U.S. Patent No. 7,039,118 as set forth below. The corrections identified herein are being submitted to correct mistakes of obvious typographical nature, and do not constitute new matter or require reexamination.

Enclosed herewith is a Certificate of Correction Form PTO/SB/44 showing the type and location of the errors to be corrected. Patentee respectfully requests that the Commissioner certify this form and return it to the undersigned counsel.

It is respectfully submitted that these are errors of the U.S. Patent and Trademark Office (Amendments filed October 27, 2005 (Attachment A) and May 26, 2005 (Attachment B) were not entered), thus no fee is required.

Please charge any shortage in fees due in the connection with the filing of this communication to Deposit Account No. **50-0206**.

Respectfully submitted,

HUNTON & WILLIAMS LLP

Date: Sept 28, 2011

By: _____

Yisun Song
Registration No. 44,487

Hunton & Williams LLP
Intellectual Property Department
2200 Pennsylvania Avenue, NW
Washington, DC 20037
(202) 955-1500 (Telephone)
(202) 778-2201 (Facsimile)

PTO/SB/44 (09-07)
Approved for use through 08/31/2010. OMB 0651-0033
U.S. Patent and Trademark Office, U.S. DEPARTMENT OF COMMERCE
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(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 7,039,118 B1

APPLICATION NO.: 09/761,211

ISSUE DATE : May 2, 2006

INVENTOR(S) : Para K. Segaram

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 2, claim 1, line 28, please delete "a media driver connectable to a transmission medium;"
Column 2, claim 1, line 29, please delete "the" and insert -- a --
Column 2, claim 1, line 31, please delete "media"
Column 2, claim 1, line 32, please delete "driver and the"
Column 2, claim 1, line 45, after "receiving the" please insert -- first differential --

Column 1, claim 4, line 14, after "ing the" please insert -- first differential --

Column 1, claim 5, line 19, please delete "input"
Column 1, claim 5, line 26, please delete "communication" and insert -- processing --

Column 1, claim 6, line 40, after "the" please insert -- serial-to-parallel --

Column 1, claim 7, line 44, after "the" please insert -- parallel-to-serial --

Column 1, claim 8, line 49, please delete "mux" and insert -- multiplexor --
Column 1, claim 8, line 50, please delete "mux" and insert -- multiplexor --

Column 1, claim 9, line 57, please delete "the" and insert -- a --

Column 1, claim 10, line 61, please delete "an internal circuit, and"
Column 1, claim 10, lines 62 and 63, please delete "a slave circuit connected to the internal circuit, the slave circuit having;"
Column 1, claim 10, line 66, please delete "millivolt" and insert "first"
Column 2, claim 10, line 4, please delete "millivolt" and insert "second"

MAILING ADDRESS OF SENDER (Please do not use customer number below): PATENT NO. 7,039,118 B1

Hunton & Williams LLP/Intellectual Property Department
2200 Pennsylvania Avenue, NW
Washington, DC 20037

PTO/SB/44 (09-07)
Approved for use through 08/31/2010. OMB 0651-0033
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.
(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO : 7,039,118 B1

APPLICATION NO.: 09/761,211

ISSUE DATE : May 2, 2006

INVENTOR(S) : Para K. Segaram

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 2, claim 11, line 11, please delete "slave" and insert -- processing --
Column 2, claim 11, line 13, please delete "input"
Column 2, claim 11, line 21, please delete "communication" and insert -- processing --

Column 2, claim 12, line 30, please delete "slave" and insert -- processing --
Column 2, claim 12, line 31, please delete "connected"
Column 2, claim 12, line 32, please delete "to the internal circuit"
Column 2, claim 12, line 34, after "the" please insert "serial-to-parallel"

Column 2, claim 13, line 35, please delete "slave" and insert -- processing --
Column 2, claim 13, line 36, please delete "connected"
Column 2, claim 13, line 37, please delete "to the internal circuit"
Column 2, claim 13, line 39, please delete "from the"
Column 2, claim 13, line 40, please delete "internal circuit"

Column 2, claim 14, line 42, please delete "slave" and insert -- processing --
Column 2, claim 14, line 43, please delete "includes" and insert -- comprises --
Column 2, claim 14, line 43, please delete "mux" and insert -- multiplexor --
Column 2, claim 14, line 44, please delete "mux" and insert -- multiplexor --

Column 2, claim 15, line 51, please delete "a media driver connectable to the transmission medium;"
Column 2, claim 15, line 53, please delete "media"
Column 2, claim 15, line 54, please delete "driver and the"
Column 2, claim 15, line 63, please delete "millivolt" and insert -- second --

Column 1, claim 18, lines 44-46, please delete ", the master clock signal and the slave clock signal having an equivalent frequency;

MAILING ADDRESS OF SENDER (Please do not use customer number below):

Hunton & Williams LLP/Intellectual Property Department
2200 Pennsylvania Avenue, NW
Washington, DC 20037

PATENT NO.: 7,039,118 B1

ATTACHMENT A

UTILITY ☒ DESIGN ☐

Application No.: 09/761,211
Inventor: Para K. Segaram
Filing Date: January 16, 2001
Atty/Sec.: TEA/vrp

Client/Matter: 57941.000032
Client: Rambus Inc.

Date: October 27, 2005

Title: HIGH SPEED COMMUNICATION SYSTEM WITH A FEEDBACK SYNCHRONIZATION LOOP

The following has been received in the U.S. Patent and Trademark Office on the date stamped hereon:

1. *Transmittal*
2. *Amendment/Response*
3. *Return Receipt Post Card*

Docketed 10/28/05

Patent Application
Attorney Docket No.: 57941.000032
Client Reference No.: RA162.CIP1.US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	:	
Para K. Segaram	:	Group Art Unit: 2631
Appln. No.: 09/761,211	:	Examiner: Kevin Michael Burd
Filed: January 16, 2001	:	
For: HIGH SPEED COMMUNICATION SYSTEM WITH A FEEDBACK SYNCHRONIZATION LOOP	:	

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL

Sir:

Submitted herewith is an Amendment/Response for the above-identified patent application.

[ ] No additional fee is required.

[X] Also attached: Terminal Disclaimer and Return Receipt Postcard.

[X] The fee is calculated as shown below:

	PRESENT # OF CLAIMS	HIGHEST # PREVIOUSLY PAID FOR	EXTRA CLAIMS	RATE	FEE
Total Claims	20	20		x $50 =	$.00
Independent Claims	5	5		x $200 =	$.00
		Multiple Dependent Claims Fee			$.00
		Terminal Disclaimer			$130.00
		Subtract ½ if Small Entity			$.00
		TOTAL FEE DUE			$130.00

[X] Please charge Deposit Account No. 50-0206 in the amount of $130.00 for the above-indicated fees. A duplicate copy of this transmittal is submitted herewith.

[X] The Commissioner is hereby authorized to charge any shortage in fees under 37 CFR 1.16 and 1.17 associated with the filing of this communication, or credit any overpayment, to Deposit Account No. 50-0206. This authorization does not include any issue fees under 37 CFR 1.18. A duplicate copy of this transmittal is submitted herewith.

Respectfully submitted,

Hunton & Williams LLP

By _____
Thomas E. Anderson
Registration No. 37,063

TEA/vrp

Hunton & Williams LLP
1900 K Street, N.W.
Washington, D.C. 20006-1109
Telephone: (202) 955-1500
Facsimile: (202) 778-2201
Date: October 27, 2005

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	
Para K. Segaram	Group Art Unit: 2631
Appln. No.: 09/761,211	Examiner: Kevin Michael Burd
Filed: January 16, 2001	
For: HIGH SPEED COMMUNICATION SYSTEM WITH A FEEDBACK SYNCHRONIZATION LOOP	

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

TERMINAL DISCLAIMER TO OBVIATE DOUBLE PATENTING REJECTION OVER A PRIOR PATENT

Sir:

The owner, Rambus Inc., of the entire interest in the instant patent application (as evidenced by the assignment recorded on January 16, 2001, at Reel 011479, Frame 0567) hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant patent application, which would extend beyond the expiration date of the full statutory term defined in 35 U.S.C. § 154 to § 156 and § 173, as presently shortened by any terminal disclaimer, of prior U.S. Patent No. 6,775,328, the entire interest in the prior patent being owned by said Rambus Inc. (as evidenced by the assignment recorded on November 26, 1999, at Reel 010405,

Frame 0583). The owner hereby agrees that any patent so granted on the instant patent application shall be enforceable only for and during such period that it and the prior patent are commonly owned. This agreement runs with any patent granted on the instant patent application and is binding upon the grantee, its successors or assigns.

In making the above disclaimer, the owner does not disclaim the terminal part of any patent granted on the instant patent application that would extend to the expiration date of the full statutory term as defined in 35 U.S.C. § 154 to § 156 and § 173 of the prior patent, as presently shortened by any terminal disclaimer, in the event that the prior patent later: expires for failure to pay a maintenance fee, is held unenforceable, is found invalid by a court of competent jurisdiction, is statutorily disclaimed in whole or terminally disclaimed under 37 C.F.R. § 1.321, has all claims canceled by a reexamination certificate, is reissued, or is in any manner terminated prior to the expiration of its full statutory term as presently shortened by any terminal disclaimer.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false

statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Please charge the $130.00 fee under 37 C.F.R. § 1.20(d) covering the cost of filing this Terminal Disclaimer to Deposit Account No. 50-0206. Any deficiency or overpayment should be charged or credited to Deposit Account No. 50-0206.

Respectfully submitted,

Hunton & Williams LLP

By: _____
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Facsimile: (202) 778-2201

Date: October 27, 2005

Patent Application
Attorney Docket No.: 57941.000032
Client Reference No.: RA162.CIP1.US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	:	
	:	
Para K. Segaram	:	Group Art Unit: 2631
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	:	Examiner: Kevin Michael Burd
Filed: January 16, 2001	:	
	:	
For: HIGH SPEED COMMUNICATION SYSTEM WITH A FEEDBACK SYNCHRONIZATION LOOP	:	

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT/RESPONSE

Sir:

In response to the Office Action dated July 27, 2005, please amend the above-identified patent application as follows:

IN THE CLAIMS:

Please amend claims 1, 4-15, and 18 as indicated in attached Appendix A.

A listing of the status of all claims 1-20 in the present patent application is provided in attached Appendix A.

REMARKS

The Office Action dated July 27, 2005, has been received and carefully considered. In this response, claims 1, 4-15, and 18 have been amended. Entry of the amendments to claims 1, 4-15, and 18 is respectfully requested. Reconsideration of the outstanding rejections in the present application is also respectfully requested based on the following remarks.

I. THE STATUTORY DOUBLE-PATENTING REJECTION OF CLAIMS 1-17

On page 3 of the Office Action, claims 1-17 were rejected under 35 U.S.C. § 101 as claiming the same invention as that of claims 1-17 of U.S. Patent No. 6,775,328. This rejection is hereby respectfully traversed with partial amendment.

Claim 1 of the present application differs in scope from claim 1 of U.S. Patent No. 6,775,328 in that claim 1 of the present application, as presently set forth, does not require a media driver connectable to a transmission medium. Accordingly, it is respectfully submitted that claim 1 of the present application, as presently set forth, does not claim the same invention as claim 1 of U.S. Patent No. 6,775,328.

Claims 2-9 of the present application are dependent upon claim 1 of the present application. Thus, claims 2-9 of the present application incorporate all limitations and the

corresponding scope of claim 1 of the present application. Accordingly, since, as discussed above, claim 1 of the present application differs in scope from claim 1 of U.S. Patent No. 6,775,328, it is respectfully submitted that claims 2-9 of the present application do not claim the same invention as claims 2-9 of U.S. Patent No. 6,775,328.

Claim 10 of the present application differs in scope from claim 10 of U.S. Patent No. 6,775,328 in that claim 10 of the present application, as presently set forth, does not require an internal circuit and a slave circuit connected to the internal circuit. Accordingly, it is respectfully submitted that claim 10 of the present application, as presently set forth, does not claim the same invention as claim 10 of U.S. Patent No. 6,775,328.

Claims 11-14 of the present application are dependent upon claim 10 of the present application. Thus, claims 11-14 of the present application incorporate all limitations and the corresponding scope of claim 10 of the present application. Accordingly, since, as discussed above, claim 10 of the present application differs in scope from claim 10 of U.S. Patent No. 6,775,328, it is respectfully submitted that claims 11-14 of the present application do not claim the same invention as claims 11-14 of U.S. Patent No. 6,775,328.

Claim 15 of the present application differs in scope from claim 15 of U.S. Patent No. 6,775,328 in that claim 15 of the present application, as presently set forth, does not require a media driver connectable to a transmission medium. Accordingly, it is respectfully submitted that claim 15 of the present application, as presently set forth, does not claim the same invention as claim 15 of U.S. Patent No. 6,775,328.

Claims 16 and 17 of the present application are dependent upon claim 15 of the present application. Thus, claims 16 and 17 of the present application incorporate all limitations and the corresponding scope of claim 15 of the present application. Accordingly, since, as discussed above, claim 15 of the present application differs in scope from claim 15 of U.S. Patent No. 6,775,328, it is respectfully submitted that claims 16 and 17 of the present application do not claim the same invention as claims 16 and 17 of U.S. Patent No. 6,775,328.

In view of the foregoing, it is respectfully requested that the aforementioned statutory double-patenting rejection of claims 1-17 be withdrawn.

II. THE NON-STATUTORY DOUBLE-PATENTING REJECTION OF CLAIMS 18 AND 19

On page 3 of the Office Action, claims 18 and 19 were rejected under the judicially created doctrine of obviousness-

type double patenting as being unpatentable over claims 18 and 19 of U.S. Patent No. 6,775,328.

A terminal disclaimer is submitted herewith to overcome the non-statutory double patenting rejection of claims 18 and 19.

In view of the foregoing, it is respectfully requested that the aforementioned non-statutory double-patenting rejection of claims 18 and 19 be withdrawn.

III. THE NON-STATUTORY DOUBLE-PATENTING REJECTION OF CLAIM 20

On page 4 of the Office Action, claim 20 was rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 20 of U.S. Patent No. 6,775,328.

A terminal disclaimer is submitted herewith to overcome the non-statutory double patenting rejection of claim 20.

In view of the foregoing, it is respectfully requested that the aforementioned non-statutory double-patenting rejection of claim 20 be withdrawn.

IV. CONCLUSION

In view of the foregoing, it is respectfully submitted that the present application is in condition for allowance, and an early indication of the same is courteously solicited. The

Examiner is respectfully requested to contact the undersigned by telephone at the below listed telephone number, in order to expedite resolution of any issues and to expedite passage of the present application to issue, if any comments, questions, or suggestions arise in connection with the present application.

To the extent necessary, a petition for an extension of time under 37 CFR § 1.136 is hereby made.

Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 50-0206, and please credit any excess fees to the same deposit account.

Respectfully submitted,

Hunton & Williams LLP

By: _____
Thomas E. Anderson
Registration No. 37,063

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Facsimile: (202) 778-2201

Date: October 27, 2005

APPENDIX A

1 (Currently Amended). A communication device comprising:

a physical layer device having:

~~a media driver connectable to a transmission medium;~~

a media receiver connectable to ~~the~~ a transmission medium;

a serializer/deserializer (serdes) connected to the ~~media driver and the~~ media receiver; and

a master circuit connected to the serdes, the master circuit having:

a first physical layer data driver, the first physical layer data driver driving a first differential signal; and

a first physical layer data receiver; and

a processing circuit having:

an internal circuit; and

a slave circuit connected to the internal circuit and the master circuit, the slave circuit having:

a first processing data receiver connected to the first physical layer data driver, the first processing data receiver outputting a first signal in response to receiving the first differential signal output from the first physical layer data driver; and

a first processing data driver connected to the first physical layer data receiver, and connectable to the first processing data receiver.

2 (Previously Presented). The device of Claim 1,

wherein the master circuit further includes a clock driver connected to the serdes, the clock driver driving a second differential signal;

wherein the slave circuit further includes a clock receiver connected to the clock driver, the clock receiver outputting a clock signal in response to a signal received from the clock driver; and

wherein the first processing data driver is connectable to receive the clock signal from the clock receiver or the first signal from the first processing data receiver, the first physical layer data receiver receiving the clock signal when the first processing data driver is connected to receive the clock signal, and the first signal when the first processing data driver is connected to receive the first signal.

3 (Original). The device of claim 2 wherein the master circuit further comprises an aligner connected to the first physical layer data receiver, the aligner receiving the clock signal when

the first physical layer data receiver receives the clock signal, the aligner receiving the first signal when the first physical layer data receiver receives the first signal, the aligner having phase comparison circuitry that compares a phase of the clock signal received by the aligner with a phase of the first signal received by the aligner to determine a phase difference.

4 (Currently Amended). The device of claim 3 wherein the master circuit further comprises a phase delay circuit connected to the aligner, the serdes, and the first physical layer data driver, the aligner passing a plurality of signal to the phase delay circuit that indicates the phase difference, the phase delay circuit delaying the first differential signal output from the first physical layer data driver so that the first signal received by the aligner is substantially in phase with the clock signal received by the aligner.

5 (Currently Amended). The device of claim 4 wherein the slave circuit further includes:

a first multiplexer connected to the clock ~~input~~ receiver and the first processing data receiver, the first multiplexer passing the clock signal output by the clock receiver when a

first mux signal is in a first logic state, and passing the first signal output by the first processing data receiver when the first mux signal is in a second logic state; and

a second multiplexer connected to the first multiplexer and the first ~~communication~~ processing data driver, the second multiplexer passing a signal output from the first multiplexer when a second mux signal is in a first logic state, and passing an output data signal when the second mux signal is in a second logic state, the signal output from the first multiplexer being the clock signal when the first mux signal is in the first logic state, and being the first signal when the first mux signal is in the second logic state.

6 (Currently Amended). The device of claim 5 wherein the slave circuit further includes a serial-to-parallel shift register connected to the clock receiver, the first processing data receiver, and the internal circuit, the clock signal output by the clock receiver clocking the serial-to-parallel shift register.

7 (Currently Amended). The device of claim 5 wherein the slave circuit further includes a parallel-to-serial shift register connected to the internal circuit, the second multiplexer, and

the clock receiver, the parallel-to-serial shift register outputting a data output signal in response to a parallel data signal from the internal circuit, the clock signal output by the clock receiver clocking the parallel-to-serial shift register.

8 (Currently Amended). The device of claim 7 wherein the slave circuit further includes a logic circuit connected to the first multiplexor, the second multiplexor, and the parallel-to-serial shift register, the logic circuit receiving the clock signal from the parallel-to-serial shift register, and setting the logic states of the first and second mux signals in response to commands extracted from the clock signal.

9 (Currently Amended). The device of claim 8 wherein the media receiver receives a signal from the transmission media having a first frequency, wherein ~~the~~ a signal output from the serdes has a second frequency, and wherein the first frequency and the second frequency are substantially equivalent.

10 (Currently Amended). A processing circuit comprising:

~~an internal circuit; and~~

~~a slave circuit connected to the internal circuit, the slave circuit having:~~

——a clock receiver connectable to a clock driver, the clock receiver outputting a clock signal in response to a first differential signal received from the clock driver;

——a first processing data receiver connectable to the first physical layer data driver, the first processing data receiver outputting a first signal in response to a second differential signal received from the first physical layer data driver; and

——a first processing data driver connectable to a first physical layer data receiver, the first processing data driver being connectable to receive the clock signal from the clock receiver or the first signal from the first processing data receiver.

11 (Currently Amended). The circuit of claim 10 wherein the ~~slave~~ processing circuit further comprises:

a first multiplexer connected to the clock ~~input~~ receiver and the first processing data receiver, the first multiplexer passing the clock signal output by the clock receiver when a first mux signal is in a first logic state, and passing the first signal output by the first processing data receiver when the first mux signal is in a second logic state; and

a second multiplexer connected to the first multiplexer and

the first ~~communication~~ processing data driver, the second multiplexer passing a signal output from the first multiplexer when a second mux signal is in a first logic state, and passing an output data signal when the second mux signal is in a second logic state, the signal output from the first multiplexer being the clock signal when the first mux signal is in the first logic state, and being the first signal when the first mux signal is in the second logic state.

12 (Currently Amended). The circuit of claim 11 wherein the ~~slave~~ processing circuit further comprises a serial-to-parallel shift register ~~connected to the internal circuit~~, the clock receiver, and the first processing data receiver, the clock signal output by the clock receiver clocking the serial-to-parallel shift register.

13 (Currently Amended). The circuit of claim 12 wherein the ~~slave~~ processing circuit further comprises a parallel-to-serial shift register ~~connected to the internal circuit~~, the second multiplexer, and the clock receiver, the parallel-to-serial shift register outputting a data output signal in response to a parallel data signal ~~from the internal circuit~~, the clock signal output by the receiver clocking the parallel-to-serial shift

register.

14 (Currently Amended). The circuit of claim 13 wherein the ~~slave~~ processing circuit further ~~includes~~ comprises a logic circuit connected to the first multiplexor, the second multiplexor, and the parallel-to-serial shift register, the logic circuit receiving the clock signal from the parallel-to-serial shift register, and setting the logic states of the first and second mux signals in response to commands extracted from the clock signal.

15 (Currently Amended). A physical layer device connectable to a transmission medium, the device comprising:

~~a media driver connectable to the transmission medium;~~

a media receiver connectable to the transmission medium;

a serializer/deserializer (serdes) connected to the ~~media driver and the~~ media receiver, the serdes outputting a master clock signal, an equivalent in-phase slave clock signal when in a calibration mode, and a data signal when in a data mode, the data signal representing a data signal received from the media receiver; and

a master circuit, the master circuit having:

a clock driver connected to output the master clock

signal as a first differential signal; and

a first physical layer data driver connectable to output the slave clock signal as a second differential signal when the serdes is in the calibration mode, and the data signal as a third differential signal when the serdes is in the data mode.

16 (Original). The device of claim 15 wherein the master circuit further includes:

a first physical layer data receiver that receives a signal which represents the master clock signal during a first phase of the calibration mode, and represents the slave clock signal during a second phase of the calibration mode; and

an aligner connected to the first physical layer data receiver, the aligner receiving the master clock signal when the first physical layer data receiver receives the master clock signal, and the slave clock signal when the first physical layer data receiver receives the slave clock signal, the aligner having phase comparison circuitry that compares a phase of the master clock signal received by the aligner with a phase of the slave clock signal received by the aligner to determine a phase difference.

17 (Original). The device of claim 16 wherein the master circuit further comprises a phase delay circuit connected to the aligner, the serdes, and the first physical layer data driver, the aligner passing a plurality of signals to the phase delay circuit that indicates the phase difference, the phase delay circuit delaying the slave clock signal output from the serdes an amount so that the slave clock signal received by the aligner is substantially in phase with the master clock signal received by the aligner when in the calibration mode, the data signal being delayed the amount when in the data mode.

18 (Previously Presented). A method for operating a communication device having a physical layer device connected to a transmission medium and a processing device connected to the physical layer device, the method comprising the steps of:

outputting a master clock signal from the physical layer device over a first path;

receiving the master clock signal in the processing device from the first path;

outputting the master clock signal as a feedback master clock signal from the processing device over a feedback path;

receiving the feedback master clock signal in the physical layer device from the feedback path;

determining a phase of the feedback master clock signal;

outputting a slave clock signal from the physical layer device over a second path after the phase of the feedback master clock signal has been determined;

receiving the slave clock signal in the processing device from the second path;

outputting the slave clock signal as a feedback slave clock signal from the processing device over the feedback path;

receiving the feedback slave clock signal in the physical layer device from the feedback path;

determining a phase of the feedback slave clock signal;

comparing the phase of the feedback master clock signal with the phase of the feedback slave clock signal to determine a phase difference; and

adjusting a delay so that the phase of the feedback slave clock signal is substantially aligned with the phase of the feedback master clock signal.

19 (Original). The method of claim 18 and further comprising the steps of:

outputting a data clock signal from the physical layer device over the first path after the phase difference has been determined;

outputting an input data signal from the physical layer device over the second path after the phase difference has been determined, the input data signal and data clock signal having an equivalent frequency; and

converting the input data signal to a parallel word by clocking the input data signal with the data clock signal.

20 (Previously Presented). A communication device comprising:

a physical layer device connectable to a transmission medium, the device having a master circuit, the master circuit having:

a clock output;

a first data output;

a first data input; and

a phase comparator connected to the first data input; and

a processing circuit having a slave circuit, the slave circuit having:

a clock input connected to the clock output;

a second data input connected to the first data output;

a second data output connected to the first data input; and

a switch for connecting an output signal from the clock input to the second data output, or an output signal from the second data input to the second data output, the phase comparator comparing a phase of the output signal from the clock input with a phase of the output signal from the second data input to determine a phase difference.

ATTACHMENT B

UTILITY ☒ DESIGN ☐

Application No.: 09/761,211
Inventor: Para K. Segaram
Filing Date: January 16, 2001
Atty/Sec.: TEA/vrp

Client/Matter: 57941.000032
Client: Rambus Inc.

Date: May 16, 2005

Title: HIGH SPEED COMMUNICATION SYSTEM WITH A FEEDBACK SYNCHRONIZATION LOOP

The following has been received in the U.S. Patent and Trademark Office on the date stamped hereon:

1. *Transmittal*
2. *Amendment/Response*
3. *Return Receipt Post Card*

DOCKETED
AP 5-17-05

Patent Application
Attorney Docket No.: 57941.000032
Client Reference No.: RA162.CIP1.US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	:	
	:	
Para K. Segaram	:	Group Art Unit: 2631
	:	
Appln. No.: 09/761,211	:	
	:	Examiner: Kevin Michael Burd
Filed: January 16, 2001	:	
	:	
For: HIGH SPEED COMMUNICATION SYSTEM WITH A FEEDBACK SYNCHRONIZATION LOOP	:	

Mail Stop Amendment
Commissioner for Patents
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TRANSMITTAL

Sir:

Submitted herewith is an Amendment/Response for the above-identified patent application.

[X] No additional fee is required.

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	PRESENT # OF CLAIMS	HIGHEST # PREVIOUSLY PAID FOR	EXTRA CLAIMS	RATE	FEE
Total Claims	20	20		x $50 =	$.00
Independent Claims	5	5		x $200 =	$.00
		Multiple Dependent Claims Fee			$.00
				Subtotal	$.00
		Subtract ½ if Small Entity			$.00
				TOTAL FEE DUE	$.00

[ ] Please charge Deposit Account No. 50-0206 in the amount of $.00 for the above-indicated fees. A duplicate copy of this transmittal is submitted herewith.

[X] The Commissioner is hereby authorized to charge any shortage in fees under 37 CFR 1.16 and 1.17 associated with the filing of this communication, or credit any overpayment, to Deposit Account No. 50-0206. This authorization does not include any issue fees under 37 CFR 1.18. A duplicate copy of this transmittal is submitted herewith.

Respectfully submitted,

Hunton & Williams LLP

By: _____
Thomas E. Anderson
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Date: May 16, 2005

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	:	
Para K. Segaram	:	Group Art Unit: 2631
Appln. No.: 09/761,211	:	Examiner: Kevin Michael Burd
Filed: January 16, 2001	:	
For: HIGH SPEED COMMUNICATION SYSTEM WITH A FEEDBACK SYNCHRONIZATION LOOP	:	

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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT/RESPONSE

Sir:

In response to the Office Action dated February 16, 2005, Applicants respectfully request favorable reconsideration of the above-identified patent application in view of the following amendments/remarks, which are believed to place the above-identified patent application in condition for allowance.

IN THE CLAIMS:

Please amend claim 18 as indicated in attached Appendix A.

A listing of the status of all claims 1-20 in the present patent application is provided in attached Appendix A.

REMARKS

The Office Action dated February 16, 2005, has been received and carefully considered. In this response, claim 18 has been amended. Entry of the amendments to claim 18 is respectfully requested. Reconsideration of the outstanding rejection in the present application is also respectfully requested based on the following remarks.

I. THE DOUBLE-PATENTING REJECTION OF CLAIMS 1-20

On page 3 of the Office Action, claims 1-20 were rejected under 35 U.S.C. § 101 as claiming the same invention as that of claims 1-20 of U.S. Patent No. 6,775,328. This rejection is hereby respectfully traversed with partial amendment.

Claims 1, 10, 15, 18, and 20 of the present application are independent claims.

Claim 1 of the present application differs in scope from claim 1 of U.S. Patent No. 6,775,328 in that claim 1 of the present application does not require the first physical layer data driver to drive a millivolt differential signal. Accordingly, it is respectfully submitted that claim 1 of the present application does not claim the same invention as claim 1 of U.S. Patent No. 6,775,328.

Claims 2-9 of the present application are dependent upon claim 1 of the present application. Thus, claims 2-9 of the present application incorporate all limitations and the corresponding scope of claim 1 of the present application. Accordingly, since, as discussed above, claim 1 of the present application differs in scope from claim 1 of U.S. Patent No. 6,775,328, it is respectfully submitted that claims 2-9 of the present application do not claim the same invention as claims 2-9 of U.S. Patent No. 6,775,328.

Claim 10 of the present application differs in scope from claim 10 of U.S. Patent No. 6,775,328 in that claim 10 of the present application does not require the clock receiver to output a clock signal in response to a millivolt differential signal. Also, claim 10 of the present application differs in scope from claim 10 of U.S. Patent No. 6,775,328 in that claim 10 of the present application does not require the first processing data receiver to output a first signal in response to a millivolt differential signal. Accordingly, it is respectfully submitted that claim 10 of the present application does not claim the same invention as claim 10 of U.S. Patent No. 6,775,328.

Claims 11-14 of the present application are dependent upon claim 10 of the present application. Thus, claims 11-14 of the

present application incorporate all limitations and the corresponding scope of claim 10 of the present application. Accordingly, since, as discussed above, claim 10 of the present application differs in scope from claim 10 of U.S. Patent No. 6,775,328, it is respectfully submitted that claims 11-14 of the present application do not claim the same invention as claims 11-14 of U.S. Patent No. 6,775,328.

Claim 15 of the present application differs in scope from claim 15 of U.S. Patent No. 6,775,328 in that claim 15 of the present application does not require the clock driver to output the master clock signal as a millivolt differential signal. Also, claim 15 of the present application differs in scope from claim 15 of U.S. Patent No. 6,775,328 in that claim 15 of the present application does not require the first physical layer data driver to output the slave clock signal as a millivolt differential signal. Accordingly, it is respectfully submitted that claim 15 of the present application does not claim the same invention as claim 15 of U.S. Patent No. 6,775,328.

Claims 16 and 17 of the present application are dependent upon claim 15 of the present application. Thus, claims 16 and 17 of the present application incorporate all limitations and the corresponding scope of claim 15 of the present application. Accordingly, since, as discussed above, claim 15 of the present

application differs in scope from claim 15 of U.S. Patent No. 6,775,328, it is respectfully submitted that claims 16 and 17 of the present application do not claim the same invention as claims 16 and 17 of U.S. Patent No. 6,775,328.

Claim 18 of the present application differs in scope from claim 18 of U.S. Patent No. 6,775,328 in that amended claim 18 of the present application does not require the master clock signal and the slave clock signal to have an equivalent frequency. Accordingly, it is respectfully submitted that amended claim 18 of the present application does not claim the same invention as claim 18 of U.S. Patent No. 6,775,328.

Claim 19 of the present application is dependent upon claim 18 of the present application. Thus, claim 19 of the present application incorporates all limitations and the corresponding scope of amended claim 18 of the present application. Accordingly, since, as discussed above, amended claim 18 of the present application differs in scope from claim 18 of U.S. Patent No. 6,775,328, it is respectfully submitted that claim 19 of the present application does not claim the same invention as claim 19 of U.S. Patent No. 6,775,328.

Claim 20 of the present application differs in scope from claim 20 of U.S. Patent No. 6,775,328 in that claim 20 of the present application does not recite a second data input

connected to the first data input, as is recited claim 20 of U.S. Patent No. 6,775,328. Accordingly, it is respectfully submitted that claim 20 of the present application does not claim the same invention as claim 20 of U.S. Patent No. 6,775,328.

In view of the foregoing, it is respectfully requested that the aforementioned double-patenting rejection of claims 1-20 be withdrawn.

II. CONCLUSION

In view of the foregoing, it is respectfully submitted that the present application is in condition for allowance, and an early indication of the same is courteously solicited. The Examiner is respectfully requested to contact the undersigned by telephone at the below listed telephone number, in order to expedite resolution of any issues and to expedite passage of the present application to issue, if any comments, questions, or suggestions arise in connection with the present application.

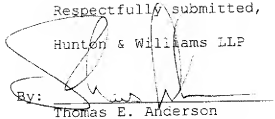
To the extent necessary, a petition for an extension of time under 37 CFR § 1.136 is hereby made.

Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to

Deposit Account No. 50-0206, and please credit any excess fees to the same deposit account.

Respectfully submitted,

Hunton & Williams LLP



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Date: May 16, 2005

APPENDIX A

1 (Previously Presented). A communication device comprising:

a physical layer device having:

a media driver connectable to a transmission medium;

a media receiver connectable to the transmission medium;

a serializer/deserializer (serdes) connected to the media driver and the media receiver; and

a master circuit connected to the serdes, the master circuit having:

a first physical layer data driver, the first physical layer data driver driving a first differential signal; and

a first physical layer data receiver; and

a processing circuit having:

an internal circuit; and

a slave circuit connected to the internal circuit and the master circuit, the slave circuit having:

a first processing data receiver connected to the first physical layer data driver, the first processing data receiver outputting a first signal in response to receiving the signal output from the first physical layer data driver; and

a first processing data driver connected to the

first physical layer data receiver, and connectable to the first processing data receiver.

2 (Previously Presented). The device of Claim 1,

wherein the master circuit further includes a clock driver connected to the serdes, the clock driver driving a second differential signal;

wherein the slave circuit further includes a clock receiver connected to the clock driver, the clock receiver outputting a clock signal in response to a signal received from the clock driver; and

wherein the first processing data driver is connectable to receive the clock signal from the clock receiver or the first signal from the first processing data receiver, the first physical layer data receiver receiving the clock signal when the first processing data driver is connected to receive the clock signal, and the first signal when the first processing data driver is connected to receive the first signal.

3 (Original). The device of claim 2 wherein the master circuit further comprises an aligner connected to the first physical layer data receiver, the aligner receiving the clock signal when the first physical layer data receiver receives the clock

signal, the aligner receiving the first signal when the first physical layer data receiver receives the first signal, the aligner having phase comparison circuitry that compares a phase of the clock signal received by the aligner with a phase of the first signal received by the aligner to determine a phase difference.

4 (Original). The device of claim 3 wherein the master circuit further comprises a phase delay circuit connected to the aligner, the serdes, and the first physical layer data driver, the aligner passing a plurality of signal to the phase delay circuit that indicates the phase difference, the phase delay circuit delaying the signal output from the first physical layer data driver so that the first signal received by the aligner is substantially in phase with the clock signal received by the aligner.

5 (Original). The device of claim 4 wherein the slave circuit further includes:

a first multiplexer connected to the clock input receiver and the first processing data receiver, the first multiplexer passing the clock signal output by the clock receiver when a first mux signal is in a first logic state, and passing the

first signal output by the first processing data receiver when the first mux signal is in a second logic state; and

a second multiplexer connected to the first multiplexer and the first communication data driver, the second multiplexer passing a signal output from the first multiplexer when a second mux signal is in a first logic state, and passing an output data signal when the second mux signal is in a second logic state, the signal output from the first multiplexer being the clock signal when the first mux signal is in the first logic state, and being the first signal when the first mux signal is in the second logic state.

6 (Original). The device of claim 5 wherein the slave circuit further includes a serial-to-parallel shift register connected to the clock receiver, the first processing data receiver, and the internal circuit, the clock signal output by the clock receiver clocking the shift register.

7 (Original). The device of claim 5 wherein the slave circuit further includes a parallel-to-serial shift register connected to the internal circuit, the second multiplexer, and the clock receiver, the shift register outputting a data output signal in response to a parallel data signal from the internal circuit,

the clock signal output by the clock receiver clocking the parallel-to-serial shift register.

8 (Original). The device of claim 7 wherein the slave circuit further includes a logic circuit connected to the first mux, the second mux, and the parallel-to-serial shift register, the logic circuit receiving the clock signal from the parallel-to-serial shift register, and setting the logic states of the first and second mux signals in response to commands extracted from the clock signal.

9 (Original). The device of claim 8 wherein the media receiver receives a signal from the transmission media having a first frequency, wherein the signal output from the serdes has a second frequency, and wherein the first frequency and the second frequency are substantially equivalent.

10 (Previously Presented). A processing circuit comprising:

an internal circuit; and

a slave circuit connected to the internal circuit, the slave circuit having:

a clock receiver connectable to a clock driver, the clock receiver outputting a clock signal in response to a first

differential signal received from the clock driver;

a first processing data receiver connectable to the first physical layer data driver, the first processing data receiver outputting a first signal in response to a second differential signal received from the first physical layer data driver; and

a first processing data driver connectable to a first physical layer data receiver, the first processing data driver being connectable to receive the clock signal from the clock receiver or the first signal from the first processing data receiver.

11 (Original). The circuit of claim 10 wherein the slave circuit further comprises:

a first multiplexer connected to the clock input receiver and the first processing data receiver, the first multiplexer passing the clock signal output by the clock receiver when a first mux signal is in a first logic state, and passing the first signal output by the first processing data receiver when the first mux signal is in a second logic state; and

a second multiplexer connected to the first multiplexer and the first communication data driver, the second multiplexer passing a signal output from the first multiplexer when a second

mux signal is in a first logic state, and passing an output data signal when the second mux signal is in a second logic state, the signal output from the first multiplexer being the clock signal when the first mux signal is in the first logic state, and being the first signal when the first mux signal is in the second logic state.

12 (Original). The circuit of claim 11 wherein the slave circuit further comprises a serial-to-parallel shift register connected to the internal circuit, the clock receiver, and the first processing data receiver, the clock signal output by the clock receiver clocking the shift register.

13 (Original). The circuit of claim 12 wherein the slave circuit further comprises a parallel-to-serial shift register connected to the internal circuit, the second multiplexer, and the clock receiver, the parallel-to-serial shift register outputting a data output signal in response to a parallel data signal from the internal circuit, the clock signal output by the receiver clocking the parallel-to-serial shift register.

14 (Original). The circuit of claim 13 wherein the slave circuit further includes a logic circuit connected to the first mux, the

second mux, and the parallel-to-serial shift register, the logic circuit receiving the clock signal from the parallel-to-serial shift register, and setting the logic states of the first and second mux signals in response to commands extracted from the clock signal.

15 (Previously Presented). A physical layer device connectable to a transmission medium, the device comprising:

a media driver connectable to the transmission medium;

a media receiver connectable to the transmission medium;

a serializer/deserializer (serdes) connected to the media driver and the media receiver, the serdes outputting a master clock signal, an equivalent in-phase slave clock signal when in a calibration mode, and a data signal when in a data mode, the data signal representing a data signal received from the media receiver; and

a master circuit, the master circuit having:

a clock driver connected to output the master clock signal as a first differential signal; and

a first physical layer data driver connectable to output the slave clock signal as a second differential signal when the serdes is in the calibration mode, and the data signal as a third differential signal when the serdes is in the data

mode.

16 (Original). The device of claim 15 wherein the master circuit further includes:

a first physical layer data receiver that receives a signal which represents the master clock signal during a first phase of the calibration mode, and represents the slave clock signal during a second phase of the calibration mode; and

an aligner connected to the first physical layer data receiver, the aligner receiving the master clock signal when the first physical layer data receiver receives the master clock signal, and the slave clock signal when the first physical layer data receiver receives the slave clock signal, the aligner having phase comparison circuitry that compares a phase of the master clock signal received by the aligner with a phase of the slave clock signal received by the aligner to determine a phase difference.

17 (Original). The device of claim 16 wherein the master circuit further comprises a phase delay circuit connected to the aligner, the serdes, and the first physical layer data driver, the aligner passing a plurality of signals to the phase delay circuit that indicates the phase difference, the phase delay

circuit delaying the slave clock signal output from the serdes an amount so that the slave clock signal received by the aligner is substantially in phase with the master clock signal received by the aligner when in the calibration mode, the data signal being delayed the amount when in the data mode.

18 (Currently Amended). A method for operating a communication device having a physical layer device connected to a transmission medium and a processing device connected to the physical layer device, the method comprising the steps of:

outputting a master clock signal from the physical layer device over a first path;

receiving the master clock signal in the processing device from the first path;

outputting the master clock signal as a feedback master clock signal from the processing device over a feedback path;

receiving the feedback master clock signal in the physical layer device from the feedback path;

determining a phase of the feedback master clock signal;

outputting a slave clock signal from the physical layer device over a second path after the phase of the feedback master clock signal has been determined~~, the master clock signal and the slave clock signal having an equivalent frequency~~;

receiving the slave clock signal in the processing device from the second path;

outputting the slave clock signal as a feedback slave clock signal from the processing device over the feedback path;

receiving the feedback slave clock signal in the physical layer device from the feedback path;

determining a phase of the feedback slave clock signal;

comparing the phase of the feedback master clock signal with the phase of the feedback slave clock signal to determine a phase difference; and

adjusting a delay so that the phase of the feedback slave clock signal is substantially aligned with the phase of the feedback master clock signal.

19 (Original). The method of claim 18 and further comprising the steps of:

outputting a data clock signal from the physical layer device over the first path after the phase difference has been determined;

outputting an input data signal from the physical layer device over the second path after the phase difference has been determined, the input data signal and data clock signal having an equivalent frequency; and

converting the input data signal to a parallel word by clocking the input data signal with the data clock signal.

20 (Previously Presented). A communication device comprising:

a physical layer device connectable to a transmission medium, the device having a master circuit, the master circuit having:

a clock output;

a first data output;

a first data input; and

a phase comparator connected to the first data input; and

a processing circuit having a slave circuit, the slave circuit having:

a clock input connected to the clock output;

a second data input connected to the first data output;

a second data output connected to the first data input; and

a switch for connecting an output signal from the clock input to the second data output, or an output signal from the second data input to the second data output, the phase comparator comparing a phase of the output signal from the clock

input with a phase of the output signal from the second data input to determine a phase difference.